WHAT IS CLAIMED IS:

1. A method for fabricating a tri-gate semiconductor device, comprising:

forming a high voltage gate dielectric layer over a semiconductor substrate;

implanting a low dose of nitrogen into said semiconductor substrate in a low voltage core region; and

forming a low voltage core gate dielectric layer over said low voltage core region, including forming an intermediate core gate dielectric layer over an intermediate core region.

2. The method as recited in Claim 1 wherein said low dose ranges from about 1E13 ions/cm^2 to about 1E14 ions/cm^2.

3. The method as recited in Claim 2 wherein said low dose ranges from about 5E13 ions/cm^2 to about 5E14 ions/cm^2.

4. The method as recited in Claim 1 wherein a thickness of said intermediate core dielectric layer is within about 0.1 nm to about 0.2 nm of a thickness of said low voltage core gate dielectric layer.

5. The method as recited in Claim 4 wherein a thickness of

said low voltage core gate dielectric layer ranges from about 0.7 nm to about 2 nm and said high voltage gate dielectric layer ranges from about 2.5 nm to about 8 nm.

6. The method as recited in Claim 1 wherein forming said low voltage core gate dielectric layer and said intermediate core dielectric layer is conducted in the presence of an environment containing nitrogen.

7. The method as recited in Claim 1 wherein said implanting includes implanting said nitrogen at an implant energy ranging from about 1 keV to about 100 keV.

8. The method as recited in Claim 1 further including forming a first gate over said high voltage gate dielectric layer, forming a second gate over said low voltage core gate dielectric layer and forming a third gate over said intermediate core dielectric layer.

9. The method as recited in Claim 8 wherein forming said second gate includes forming said second gate such that a concentration of nitrogen within said second gate is substantially uniform throughout said second gate.

10. A method for manufacturing a tri-gate integrated circuit, comprising:

forming high voltage gate dielectric layers over a semiconductor substrate;

implanting a low dose of nitrogen into said semiconductor substrate in low voltage core regions; and

forming core gate dielectric layers over said low voltage core regions, including forming intermediate core gate dielectric layers over intermediate core regions;

forming first transistor gates over said high voltage gate dielectric layers, second transistor gates over said low voltage core gate dielectric layers and third transistor gates over said intermediate core dielectric layers;

forming source/drain regions associated with each of said first, second and third transistor gates; and

forming interconnects extending through dielectric layers located over first, second and third transistor gates to interconnect said first, second and third transistor gates to form an operative tri-gate integrated circuit.

11. The method as recited in Claim 1 wherein said low dose ranges from about 5E13 ions/cm^2 to about 5E14 ions/cm^2.

12. The method as recited in Claim 10 wherein a thickness of

said intermediate core dielectric layers are within about 0.1 nm to about 0.2 nm of a thickness of said core gate dielectric layers.

13. The method as recited in Claim 12 wherein a thickness of said low voltage core gate dielectric layers range from about 0.7 nm to about 2 nm and said high voltage gate dielectric layer ranges from about 2.5 nm to about 8 nm.

14. The method as recited in Claim 10 wherein forming said low voltage core gate dielectric layer and said intermediate core dielectric layers is conducted in the presence of a plasma environment containing nitrogen.

15. The method as recited in Claim 10 wherein said implanting includes implanting said nitrogen at an implant energy ranging from about 1 keV to about 100 keV.

16. The method as recited in Claim 10 wherein forming said second gates includes forming said second gates such that a concentration of nitrogen within each of said second gates is substantially uniform throughout said second gates.

17. The method as recited in Claim 16 wherein an atomic percentage of said nitrogen varies by about 1 percent throughout

each of said second gates.

18. An tri-gate semiconductor device, comprising:

a semiconductor substrate;

a first gate located over said semiconductor substrate and over a high voltage gate dielectric within a high voltage region;

a second gate located over said semiconductor substrate and over a low voltage gate dielectric within a low voltage core region;

a third gate located over said semiconductor substrate and over an intermediate core oxide within an intermediate core region;

source/drains formed within said semiconductor substrate and associated with each of said first, second and third gates; and

interconnects formed within dielectric layers located over said first, second and third gates that interconnect said first, second and third gates and said source/drains to form an operative tri-gate integrated circuit.

19. The tri-gate semiconductor device as recited in Claim 18 wherein said semiconductor substrate further includes a concentration of nitrogen near a surface thereof within said low voltage core region.

20. The tri-gate semiconductor device as recited in Claim 19 wherein said low concentration of nitrogen ranges from about 1E18 ions/cm^2 to about 1E21 ions/cm^2.

21. The tri-gate semiconductor device as recited in Claim 19 wherein an atomic percentage of nitrogen within said second gate varies by about less than 1 percent throughout said second gate.

22. The tri-gate semiconductor device as recited in Claim 18 wherein a thickness of said intermediate core gate dielectric is within about 0.1 nm to about 0.2 nm of a thickness of said low voltage gate dielectric.

23. The tri-gate semiconductor device as recited in Claim 18 wherein an operating voltage of said second gate is substantially the same as an operating voltage of said third gate.

24. The tri-gate semiconductor device as recited in Claim 23 wherein said second gate is configured to operate at a voltage ranging from about 0.7 volts to about 1.5 volts and said third gate is configured to operate at a voltage ranging from about 0.8 volts to about 1.5 volts.

25. The tri-gate semiconductor device as recited in Claim 24 wherein said first gate is configured to operate at a voltage ranging from about 1 volt to about 5 volts.